CLAIMS

1. A method of designing a logic circuit to provide a predetermined logical operation, the method including the steps of:

(a) defining a logic synthesis block comprising a dynamic logic circuit;

(b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, the logic synthesis being performed utilizing a synthesis library constrained to the logic synthesis block;

(c) eliminating unused devices in the intermediate circuit to produce a final circuit; and

(d) sizing the devices in the final circuit.

2. The method of Claim 1 wherein the step of defining the logic synthesis block includes selecting the largest practical dynamic AND/OR circuit for the integrated circuit fabrication technology in which the circuit is to be implemented.

3. The method of Claim 2 wherein the logic synthesis block comprises a four high and four wide dynamic AND/OR circuit.

4. The method of Claim 1 wherein the step of performing logic synthesis includes leaving the size of the devices in the logic synthesis block substantially unconstrained.

5. The method of Claim 1 wherein the step of eliminating unused devices from the intermediate circuit includes detecting devices having a state that remains constant as the intermediate circuit operates to provide the predetermined logical operation.

6. The method of Claim 1 wherein the step of sizing the devices in the final circuit includes analyzing the final circuit to determine the characteristics of each device in the final circuit necessary in order to consistently provide the predetermined logical operation and meet drive requirements.

7. The method of Claim 1 wherein the logic synthesis block uses a single activation/reset clock signal.

8. A method of synthesizing a logic circuit to provide a predetermined logical operation, the method including the steps of:

(a) defining a logic synthesis block comprising a dynamic logic circuit; and

(b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, the logic synthesis utilizing a synthesis library constrained to the dynamic logic circuit comprising the logic synthesis block.

9. The method of Claim 8 wherein the step of defining the logic synthesis block includes selecting the largest practical dynamic AND/OR circuit for the fabrication technology in which the circuit for performing the predetermined logical operation is to be implemented.

10. The method of Claim 8 wherein the logic synthesis block comprises a four high and four wide dynamic AND/OR circuit.

11. The method of Claim 8 wherein the step of performing logic synthesis for the predetermined logical operation includes leaving device size in the logic synthesis block substantially unconstrained.

12. The method of Claim 8 wherein the dynamic logic circuit comprising the logic synthesis block operates using a single activation/reset clock signal.

13. In a circuit design method utilizing a logic synthesis tool and predefined logic circuit library to provide a logic implementation for a predetermined logical operation, the improvement comprising:

(a) defining a logic synthesis block comprising a dynamic logic circuit; and

(b) constraining the logic synthesis tool to the logic synthesis block.

14. The method of Claim 13 wherein the logic synthesis tool produces an intermediate circuit design which performs the predetermined logical operation, and further including the steps of:

(a) eliminating unused devices in the intermediate circuit design to produce a final circuit; and

(b) sizing the devices in the final circuit.

15. The method of Claim 13 wherein the step of defining the logic synthesis block includes selecting the largest practical dynamic AND/OR circuit for the circuit fabrication technology in which the circuit design is to be implemented.

16. The method of Claim 13 wherein the logic synthesis block comprises a four high and four wide dynamic AND/OR circuit.

17. The method of Claim 13 further including the step of leaving the device size in the logic synthesis block substantially unconstrained for the logic synthesis tool.

18. The method of Claim 13 wherein the logic synthesis block uses a single activation/reset clock input.